REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested. New claims 21 and 22 are added, and Claims 1-22 are pending in the application.

Applicant hereby amends the application as required to perfect the priority claim under 35 USC §119 and 37 CFR §1.78(a)(5). Since the subject application was filed before November 29, 2000, the time periods of 37 CFR §1.78(a)(5)(ii) do not apply. See 37 CFR §1.78(a)(5)(ii)(A).

The specification also has been amended at pages 5 and 7 to correct informalities. A marked-up version of the amendments is attached, where insertions are underlined and deletions are bracketed.

Claims 1-6, 10-13, 17-18 and 20 stand rejected under 35 USC §102(e) in view of U.S. Patent No. 6, 115,385 to Vig. This rejection is respectfully traversed. The following is a comparison between the independent claims and the applied reference.

Each of the independent claims 1, 10 and 17 specify an integrated network switch having a switching module and configured for switching a layer 2 data packet within a network having a plurality of subnetworks. Moreover, each of the independent claims 1, 10, and 17 specifies that the switching module includes a plurality of address tables for storing the layer 3 switching information for the respective subnetworks, where each address table is configured for storing host identifiers for a corresponding subnetwork.

For example, claim 1 specifies "storing address information from the layer 2 packet, including the host identifier, in a selected one of a plurality of address tables within the switching module based on the corresponding subnetwork identifier, each of the address tables configured

for storing the host identifiers of respective transmitting nodes of a corresponding one of the subnetworks".

Claim 10 specifies "selecting one of a plurality of address tables within the switching module based on the corresponding subnetwork identifier, each of the address tables configured for storing the host identifiers of respective transmitting nodes of a corresponding one of the subnetworks".

Claim 17 specifies "a switching module ... including a plurality of address tables for storing the layer 3 switching information for the respective subnetworks, the switching module accessing a selected one of the address tables based on the corresponding subnetwork identifer...."

Hence, search times for layer 3 switching information can be dramatically reduced by providing a plurality of address tables that can be independently accessed by the switching logic on a per-subnetwork basis. These and other features are neither disclosed nor suggested in the applied prior art.

Vig discloses in Figure 3 a switch 30 that is configured for switching packets between a first IP subnet 32 and a second IP subnet 34.

However, Vig discloses that a single subnet may be served by multiple switch ports, hence Vig uses a single table for all subnet-to-port mapping. For example, Vig specifies at col. 3, lines 12-16: "[t]he switch builds a subnet to port mapping table based on packets received from each source host and selectively forwards the multicast packet to all ports on which the destination subnet is active."

Further, as described at column 8, line 51 to column 9, line 2, Vig relies on a single table for all subnet-to-port mapping:

> Next, in decision step 814, a test is made to determine if a source subnet is defined in a [sic] internal subnet to port mapping table by the switch CPU. If the source subnet is not defined, then processing proceeds to decision step 822. If the source subnet is defined, then in decision step 816, a test is made to determine if the source subnet is allowed on the source port. If it is not, then the packet is discarded in step 818. If the source subnet is allowed on the source port, the switch CPU logic, in step 820, adds the source port to the list of ports on which the source subnet is active as indicated in the subnet to port mapping table.
>
> The final stage of processing in FIGS. 8A-8B tests for destination subnet. In decision step 822, a test is performed to determine if the destination subnet is defined in the internal subnet to port mapping table. If the destination subnet is not defined, all ports are flooded except for the source port in step 824. Otherwise switch CPU logic forwards the packet to all ports on which the destination subnet is active as indicated in the subnet to port mapping table.

Applicant traverses the assertion in the Official Action that col. 6, lines 39-40 discloses the claimed plurality of address tables: col. 6, lines 39-40 reads "[t]he switch learns MAC addresses and keeps internal tables that map MAC addresses to switch ports." This portion of Vin is describing layer 2 MAC addresses, and not storage of layer 3 host identifiers, as claimed. Further, the cited portion neither discloses nor suggests "each of the address tables configured for storing the host identifiers ... of a corresponding one of the subnetworks," as claimed.

Further, col. 8, lines 8-12 reads "... those packets with destination layer-2 address C0 00 FF FF FF FF must be forwarded to the switch CPU. The CPU can then analyze the packet and selectively forward it to a subset of switch ports based on layer-3 information like destination subnet as illustrated in FIG. 6." Hence, Vin teaches that the CPU performs processing of the layer 3 information, but neither discloses nor suggests the claimed plurality of address tables, let

alone where each address table is configured for storing host identifiers of a corresponding subnetwork.

Hence, the independent claims are distinguishable in that Vig neither discloses nor suggests a plurality of address tables within the switching module, where each address table is configured for storing host identifiers for a corresponding one of the subnetworks, as claimed.

For these and other reasons, the §102 rejection of independent claims 1, 10, and 17 should be withdrawn.

It is believed claims 2-6, 11-13, 18 and 20 are patentable in view of their dependency from their independent claims. Further, Applicant traverses the rejection of claims 3-4 and 12-13: as apparent from the foregoing, Vig teaches that a single subnetwork may be served by multiple switch ports. Hence, Vig neither discloses nor suggests that each network switch port is connected to a corresponding subnetwork, let alone that each address table is assigned to a corresponding one network switch port, as claimed. Hence, these claims are further patentable over Vig.

Claims 7-9, 14-16, and 19 stand rejected under 35 USC §103 in view of Vig and U.S. Patent No. 6,529,503 to Chiang et al. As described below in the Statement of Common Ownership, Chiang et al. is not available as a reference under §103(c). Hence, this §103 rejection should be withdrawn.

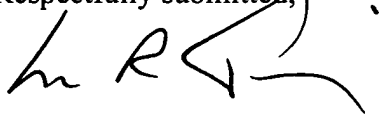
STATEMENT OF COMMON OWNERSHIP:

At the time the invention claimed in the subject application was made, the subject application 09/482,956 and U.S. Patent No. 6,529,503 to Chiang et al. were owned by, or subject to an obligation of assignment to, the same entity (Advanced Micro Devices, Inc. of Sunnyvale, California).

In view of the above, it is believed this application is and condition for allowance, and such a Notice is respectfully solicited.

To the extent necessary, Applicant petitions for an extension of time under 37 C.F.R. 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including any missing or insufficient fees under 37 C.F.R. 1.17(a), to Deposit Account No. 50-0687, under Order No. 95-309, and please credit any excess fees to such deposit account.

Respectfully submitted,



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MARKED-UP VERSION OF AMENDMENTS

Amendment to paragraph starting at page 5, line 19:

Moreover, the switch fabric 25 is configured to include multiple address tables that are configured to optimize lookup times for address entries. Specifically, each address table 30 is configured for storing the layer 2 and layer 3 switching information for the corresponding subnetwork 18. Hence, the switch module 25, under the control of switching logic 32, accesses a selected one of the address tables 30 based on the corresponding subnetwork identifier. The switching module 25 can then search within the selected address table (e.g., 30a) for the layer 3 switching information of the received layer 2 data packet based on the corresponding host identifier. Hence, search times can be dramatically reduced by providing a plurality of address tables 30 that can be independently accessed by the switching logic 32 on a per-subnetwork [bases] basis. As illustrated in Figure 1, each of the address tables 30 are assigned to the corresponding one of the network switch ports 20, enabling each network switch port to handle a corresponding subnetwork 18. Hence, the switching logic 25 is capable of providing lookup processing for each of the ports 20 simultaneously and in parallel, merely by identifying the table by the subnet identifier supported by the corresponding switch port 20.

Amendments to paragraph starting at page 7, line 23:

If the switching logic 32 [is] does not find the table entry in step 58, then the switching logic 32 stores in step 60 address information from the layer 2 packet, including the host identifier 46, the MAC address, and any virtual LAN (VLAN) association information to be used for learning operations. However if the switching logic 32 does [funny] find the table entry [instead] in step 58, then the switching logic 32 fetches the layer 3 switching information in step 62.